In the Drawings

The lettering in the drawings have been enlarged to measure at least 1/8 inch height. Replacement formal drawings are attached herewith.

In the Claims

Amend claims 1, 3 and 4 as follows:

1. (Currently Amended) A method, comprising:

identifying at least one electrical characteristic for an alpha device;
identifying the at least one electrical characteristic for a plurality of dependent devices; and
identifying a group comprising the alpha device and the plurality of dependent devices comprising the at least one electrical characteristic for associated manufacturing testing.

2. (Original) The method of claim 1, further comprising grouping the alpha device and the plurality of dependent devices together on a semiconductor device for the associated manufacturing testing.

3. (Currently Amended) The method of claim 2, wherein said grouping comprises electrically connecting the alpha device to the plurality of dependent devices during the associated manufacturing testing.

4. (Currently Amended) The method of claim 3, further comprising electrically disconnecting the alpha device from the plurality of dependent devices upon completion of the associated manufacturing testing.

5. (Original) The method of claim 2, further comprising providing by the alpha device, a first signal adapted to operate the plurality of dependent devices during the associated manufacturing testing.

6. (Original) The method of claim 5, further comprising providing a second signal adapted to operate the plurality of dependent devices during the associated manufacturing testing; and
multiplexing between the first signal and the second signal during the associated manufacturing testing.

7. (Original) The method of claim 2, further comprising testing the plurality of dependent devices simultaneously in parallel during the associated manufacturing testing.

8. (Original) The method of claim 2, further comprising testing the plurality of dependent devices individually during the associated manufacturing testing.

9. (Original) The method of claim 2, wherein the alpha device and the plurality of dependent devices are cores on the semiconductor device.

10. (Original) The method of claim 2, wherein the semiconductor device is an application specific integrated circuit (ASIC).

11. (Original) The method of claim 1, wherein the at least one electrical characteristic comprises an operational frequency of the plurality of dependent devices.

12. (Original) The method of claim 11, wherein the operational frequency comprises a range of about 1 gigahertz to about 6 gigahertz.

13. (Original) The method of claim 1, wherein the at least one electrical characteristic comprises a jitter tolerance of the plurality of dependent devices.

14. (Original) The method of claim 1, wherein the alpha device comprises a phase lock loop circuit.

15. (Original) The method of claim 14, wherein each of the plurality of dependent devices comprise a serializer/deserializer (SerDes) circuit.

16. (Original) The method of claim 1, wherein the associated manufacturing testing comprises testing the plurality of dependent device for functional operation.

17. (Original) The method of claim 16, wherein the associated manufacturing testing comprises testing the plurality of dependent devices for the functional operation within a design specification.

18. (Original) The method of claim 17, wherein the design specification is a frequency range.

19. (Original) The method of claim 17, wherein the design specification is a speed at which the plurality of dependent devices perform the functional operation.

20. (Original) The method of claim 1, wherein the plurality of dependent devices is selected from the group consisting of an analog to digital convertor, a digital to analog convertor, and a BIST engine.